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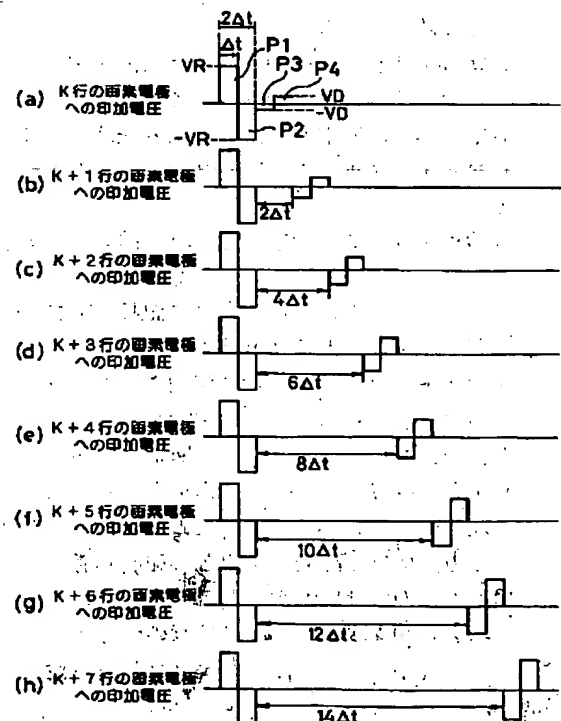
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(54)【発明の名称】 強誘電性液晶表示装置及び強誘電性液晶表示素子の駆動方法

(57)【要約】

【目的】 DHF液晶を用いたアクティブマトリクスタイプの強誘電性液晶表示素子に、明確な階調表示を行なわせ、しかも、書き込み時間を短くする。

【構成】 各行の画素の選択期間を前期選択期間と後期選択期間に分割する。前期選択期間には、DHF液晶の螺旋構造を解くために十分な電圧 $-VR$ と、この電圧と逆極性で絶対値が等しい電圧 $VR$ を所定の順番で液晶に印加し、表示素子をブランキング状態に設定する。後期選択期間には、補償電圧 $-VD$ と書き込み電圧 $VD$ を液晶に順番に印加し、画素の階調を表示階調に設定する。書き込み電圧 $VD$ は、表示階調に応じて変化し、補償パルスは書き込み電圧 $VD$ と逆極性で絶対値が等しい電圧である。前期選択期間は複数行の画素に同一のタイミングで設定され、後期選択期間は、行毎に異なったタイミングで設定される。



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## 【特許請求の範囲】

【請求項 1】画素電極と画素電極に接続された薄膜トランジスタがマトリクス状に複数配列された一方の基板と、前記画素電極に対向する対向電極が形成された他方の基板と、これらの基板の間に配置され、層構造と前記基板の間隔より小さい螺旋ピッチの螺旋構造をもち、前記画素電極と対向電極間に印加された電圧に応じて液晶分子が一方の方向にほぼ配列した第 1 の配向状態と、液晶分子が他方の方向にほぼ配列した第 2 の配向状態と、前記螺旋構造の歪みにより液晶分子の平均的な配列方向が前記一方の方向と他方の方向の間となる中間の配向状態にそれぞれ配向する非メモリー性強誘電性液晶、を備えた強誘電性液晶表示素子の駆動方法において、前記画素電極と対向電極とそれらに挟まれた前記強誘電性液晶から構成される各画素の選択期間は、前期選択期間と後期選択期間を含み、

前記前期選択期間を前記マトリクスの複数の行で同一タイミングとし、前記液晶を前記第 1 の配向状態と第 2 の配向状態の少なくとも一方の状態に設定する初期化電圧を前記画素電極と前記対向電極間に印加し、前記後期選択期間には、前記マトリクスの行毎に異なったタイミングとし、表示階調に応じて変化する書き込み電圧を前記画素電極と前記対向電極間に印加する、ことを特徴とする強誘電性液晶表示素子の駆動方法。

【請求項 2】前記初期化電圧は、前記強誘電性液晶を第 1 の配向状態に配向させる第 1 のパルスと、前記強誘電性液晶を第 2 の配向状態に配向させる第 2 のパルスを含む、ことを特徴とする請求項 1 記載の駆動方法。

【請求項 3】前記第 1 と第 2 のパルスは、極性が反対で、絶対値が等しい電圧を有することを特徴とする請求項 2 記載の駆動方法。

【請求項 4】前記後期選択期間に前記書き込み電圧と、前記書き込み電圧と極性が逆でかつ絶対値が等しい補償電圧を前記画素電極と前記対向電極間に印加することを特徴とする請求項 1 ないし 3 のいずれか 1 つに記載の駆動方法。

【請求項 5】前記初期化電圧は、前記液晶表示素子の表示を黒状態に設定する電圧であることを特徴とする請求項 1 ないし 4 のいずれか 1 つに記載の駆動方法。

【請求項 6】画素電極と該画素電極に接続されたアクティブ素子がマトリクス状に配列された一方の基板と、前記画素電極に対向する対向電極が形成された他方の基板と、前記基板間に配置され、層構造と前記基板の間隔より小さい螺旋ピッチの螺旋構造をもち、前記画素電極と前記対向電極間に印加された電圧に応じて液晶分子が一方の方向にほぼ配列した第 1 の配向状態と、液晶分子が他方の方向にほぼ配列した第 2 の配向状態と、前記第 1 と第 2 の配向状態の中間の任意の配向状態に配向する非メモリー性強誘電性液晶、を備えた強誘電性液晶表示素子と、

前記アクティブ素子に接続され、前記画素電極を前期選択期間と前記前期選択期間と異なるタイミングの後期選択期間で選択し、前記前期選択期間には、前記強誘電性液晶を前記第 1 または第 2 の配向状態の一方に設定するための電圧を前記アクティブ素子を介して前記マトリクスの複数の行の前記画素電極に印加し、後期選択期間には、画素の表示階調に応じて変化する電圧を前記アクティブ素子を介して前記画素電極に印加する駆動手段、を備えることを特徴とする強誘電性液晶表示装置。

10 【請求項 7】前記アクティブ素子は電流路の一端が対応する画素電極に接続された薄膜トランジスタから構成され、

前記駆動手段は、

対応する行の複数の前記薄膜トランジスタのゲートに接続されたゲートラインと、

対応する列の複数の前記薄膜トランジスタの電流路の他端に接続されたデータラインと、

20 前記前期選択期間及び前記後期選択期間に、その行の前記ゲートラインに前記薄膜トランジスタをオンさせるゲート電圧を供給する行駆動手段と、

前記前期選択期間に、前記強誘電性液晶を前記第 1 または第 2 の配向状態の一方に設定するための初期化電圧を前記データラインに印加し、前記後期選択期間に、前記表示階調に対応した書き込み電圧を前記データラインに印加する列駆動手段、を備える、ことを特徴とする請求項 6 記載の強誘電性液晶表示装置。

【請求項 8】前記前期選択期間に、前記行駆動手段は、複数の前記ゲートラインに同時にゲート電圧を印加し、前記列駆動手段は、前記初期化電圧を前記データラインに印加し、

前記後期選択期間に、前記行駆動手段は前記後期選択期間に前記ゲート電圧を異なったタイミングで前記ゲートラインに印加し、前記列駆動手段は前記書き込み電圧を前記データラインに印加する、ことを特徴とする請求項 7 記載の強誘電性液晶表示装置。

【請求項 9】前記列駆動手段は、前記前期選択期間において、前記強誘電性液晶を第 1 の配向状態に設定する第 1 のパルスと前記強誘電性液晶を第 2 の配向状態に設定する第 2 のパルスを前記データラインに印加する、ことを特徴とする請求項 7 または 8 記載の強誘電性液晶表示装置。

【請求項 10】前記第 1 のパルスと第 2 のパルスは、極性が反対で絶対値が等しい電圧を有することを特徴とする請求項 9 記載の強誘電性液晶表示装置。

【請求項 11】前記列駆動手段は、前記後期選択期間に、前記書き込み電圧と共に前記書き込み電圧と逆極性でかつ絶対値が等しい補償電圧を前記データラインに印加する、ことを特徴とする請求項 7 ないし 10 のいずれか 1 つに記載の強誘電性液晶表示装置。

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【請求項12】前記駆動手段は、前記前期選択期間において、前記強誘電性液晶表示素子を暗状態に設定することを特徴とする請求項6ないし11のいずれか1つに記載の強誘電性液晶表示装置。

【発明の詳細な説明】

【0001】

【産業上の利用分野】この発明は、強誘電性液晶の一種であるDHF (Deformed Helix Ferroelectric) 液晶を用いた液晶表示装置及び液晶表示素子の駆動方法に関し、特に、階調表示可能でかつ書き込み時間の短いDHF液晶表示装置及びDHF液晶表示素子の駆動方法に関する。

【0002】

【従来の技術】強誘電性液晶を用いる強誘電性液晶表示素子は、ネマティック液晶を用いるTNモードの液晶表示素子と比較して、高速応答、広い視野角が得られる等の点で注目されている。

【0003】この強誘電性液晶表示素子の実用化に関する研究は、従来、SS-F液晶と呼ばれる、カイラルスメクティックC相の螺旋ピッチが液晶素子の基板間隔（セルギャップ）より大きくかつ配向状態のメモリ性（双安定性）を有する強誘電性液晶を対象として行なわれていた。

【0004】上記SS-F液晶を用いる強誘電性液晶表示素子は、SS-F液晶をその螺旋構造を消失させた状態で基板間に封入したもので、印加電圧と液晶の自発分極との相互作用により、一方の電極の電圧を印加したときの第1の配向状態と他方の極性の電圧を印加したときの第2の配向状態との2つの配向状態を得、この液晶の配向状態と素子の入射側と出射側とに配置した一対の偏光板とにより光の透過率を制御して表示する。

【0005】しかし、上記SS-F液晶を用いる強誘電性液晶表示素子は、液晶の配向状態が第1の配向状態と第2の配向状態との2つの状態だけであり、電圧無印加状態でもいずれかの配向状態が維持されるため、透過率を変化させて階調のある表示を行なわせることは難しいとされている。

【0006】そこで、最近では、階調表示の可能な強誘電性液晶表示素子の開発が研究されており、「LIQUID CRYSTALS」, 1989, Vol.5, NO.4, の第1171頁ないし第1177頁に記載されているように、カイラルスメクティックC相の螺旋ピッチが表示素子の基板間隔より小さくかつ配向状態のメモリ性を有さない強誘電性液晶を用いることが提案されている。この強誘電性液晶は、上記SS-F液晶と区別してDHF液晶と呼ばれている。

【0007】DHF液晶を用いる強誘電性液晶表示素子では、DHF液晶が螺旋構造をもった状態で基板間に封入されている。液晶層を挟んで対向する電極間に印加される電圧に応じて、DHF液晶は、液晶分子の長軸方向（ダイレクタ）が第1の方向にほぼ配列した第1の配向

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状態、液晶分子の長軸方向が第2の方向にほぼ配向した第2の配向状態、または、液晶分子の長軸方向の平均的な配列が前記第1と第2の方向の間の任意の方向となる中間配向状態に設定される。

【0008】DHF液晶は、上記SS-F液晶と異なり、配向状態のメモリ性は有していないが、中間配向状態をとることができるので、非選択期間中も中間配向状態を維持するようにすれば、階調表示が可能である。

【0009】この強誘電性液晶表示素子に階調表示を行なわせる駆動方法としては、従来、各画素の選択期間（書き込み期間）に表示すべき階調に応じた電圧（書き込み電圧）を各画素に印加する方法が考えられている。

【0010】しかし、上記の駆動方法では、書き込み電圧と画素の透過率とが対応せず、階調の制御がほとんど不可能で、実用レベルの階調表示を実現することはできなかった。これは、一般に、DHF液晶の光学特性（印加電圧と透過率の関係）はヒステリシスが大きく、単純に表示階調に対応する電圧をDHF液晶に印加しても、それ以前に印加された電圧との関係で、階調が一義的に定まらないためである。

【0011】このような問題を解決するため、特願平4-327002には、選択期間毎にDHF液晶を一旦第1の配向状態と第2の配向状態の一方に設定するための初期化電圧をDHF液晶に印加し、その後、表示データに応じた書き込み電圧を印加する駆動方法が開示されている。

【0012】この駆動方法では、各行の画素の選択期間に、画素電極に4つのパルスを印加する。すなわち、書き込みパルスと逆極性で電圧値の絶対値が同一の補償パルス、極性が異なるが絶対値が同一の第1と第2のリセットパルス、表示階調に対応する電圧を有する書き込みパルスを順次印加し、書き込みパルスを印加している際、アクティブ素子をオンする。

【0013】このような構成によれば、第1と第2のリセットパルスにより、DHF液晶が螺旋構造が解けた状態に設定され、その後、書き込みパルスの電圧が各画素に非選択期間の間保持される。従って、書き込み電圧に対応する階調が一義的に定まると共にその階調が1フレームの間維持され、階調表示が可能となる。また、第1と第2のリセットパルス、書き込みパルスと補償パルスがそれぞれ相殺されるため、DHF液晶に印加される電圧に直流成分は発生しない。

【0014】

【発明が解決しようとする課題】前述したように、従来のDHF液晶素子の駆動方法では、表示階調が一義的に定まらず、実質的に、階調表示ができないという問題があった。また、特願平4-327002に開示された駆動方法では、印加電圧が直流成分を含まないようにするため、リセットパルスと書き込みパルスに加えて、2つの補正パルスを必要とする。このため、各選択期間に同

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一内容でビットを反転したデータを2回ドライバに転送する必要があり、表示制御及びドライバの構成が複雑であった。また、選択期間毎に4つのパルスデータをデータラインに印加する必要があり、選択期間が長くなり、その結果、1画面分の書き込み期間が長くなるという問題もあった。

【0015】この発明は上記実状に鑑みてなされたもので、表示制御系の構成が比較的簡単で、また、1画面の書き込み時間の短縮化を可能にするDHF液晶表示素子の階調表示方法及びDHF液晶表示装置を提供することを目的とする。また、この発明は基板間隔より小さい螺旋ピッチをもち、印加する電圧に応じて第1の配向状態と第2の配向状態及び中間の任意の配向状態にそれぞれ配向する非メモリ性強誘電性液晶(DHF)液晶を用いたアクティブマトリクス方式の強誘電性液晶表示素子に、明確な階調表示を行なわせることができ、しかも、書き込み時間の短い液晶表示素子の駆動方法及び液晶表示装置を提供することを目的とする。

【0016】

【課題を解決するための手段】上記目的を達成するため、この発明にかかる強誘電性液晶表示素子の駆動方法は、画素電極と画素電極に接続された薄膜トランジスタがマトリクス状に複数配列された一方の基板と、前記画素電極に対向する対向電極が形成された他方の基板と、これらの基板の間に配置され、層構造と前記基板の間隔より小さい螺旋ピッチの螺旋構造をもち、前記画素電極と対向電極間に印加された電圧に応じて液晶分子が一方の方向にほぼ配列した第1の配向状態と、液晶分子が他方の方向にほぼ配列した第2の配向状態と、前記螺旋構造の歪みにより液晶分子の平均的な配列方向が前記一方の方向と他方の方向の間となる中間の配向状態にそれぞれ配向する非メモリ性強誘電性液晶、を備えた強誘電性液晶表示素子の駆動方法において、前記画素電極と対向電極とそれらに挟まれた前記強誘電性液晶から構成される各画素の選択期間は、前期選択期間と後期選択期間を含み、前記前期選択期間を前記マトリクスの複数の行で同一タイミングとし、前記液晶を前記第1の配向状態と第2の配向状態の少なくとも一方の状態に設定する初期化電圧を前記画素電極と前記対向電極間に印加し、前記後期選択期間には、前記マトリクスの行毎に異なったタイミングとし、表示階調に応じて変化する書き込み電圧を前記画素電極と前記対向電極間に印加する、ことを特徴とする。

【0017】上記目的を達成するため、この発明にかかる強誘電性液晶表示装置は、画素電極と該画素電極に接続されたアクティブ素子がマトリクス状に配列された一方の基板と、前記画素電極に対向する対向電極が形成された他方の基板と、前記基板間に配置され、層構造と前記基板の間隔より小さい螺旋ピッチの螺旋構造をもち、前記画素電極と前記対向電極間に印加された電圧に応じ

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て液晶分子が一方の方向にほぼ配列した第1の配向状態と、液晶分子が他方の方向にほぼ配列した第2の配向状態と、前記第1と第2の配向状態の中間の任意の配向状態に配向する非メモリ性強誘電性液晶、を備えた強誘電性液晶表示素子と、前記アクティブ素子に接続され、前記画素電極を前期選択期間と前記前期選択期間と異なるタイミングの後期選択期間で選択し、前記前期選択期間には、前記強誘電性液晶を前記第1または第2の配向状態の一方に設定するための電圧を前記アクティブ素子を介して前記マトリクスの複数行の前記画素電極に印加し、後期選択期間には、画素の表示階調に応じて変化する電圧を前記アクティブ素子を介して前記画素電極に印加する駆動手段、を備えることを特徴とする。

【0018】上記構成において、初期化電圧は、液晶を第1の配向状態に設定する第1のパルスと、第2の配向状態に設定する第2のパルスを含み、前記第1と第2のパルスの電圧の絶対値は等しい。

【0019】後期選択期間に、書き込み電圧と極性が逆でかつ絶対値が等しい補償電圧を前記液晶に印加するようにしてもよい。アクティブ素子は、例えば、薄膜トランジスタから構成される。また、駆動手段は、例えば、対応する行の前記前期選択期間及び前記後期選択期間に、対応する前記ゲートラインに前記薄膜トランジスタをオンさせる信号を供給する行駆動手段と、前期選択期間に、前記液晶分子を前記第1または第2の配向状態の一方に設定するための初期化電圧を薄膜トランジスタを介して画素電極に印加し、後期選択期間に、前記表示階調に対応した書き込み電圧を薄膜トランジスタを介して画素電極に印加する列駆動手段、から構成される。

【0020】

【作用】上記構成によれば、初期化電圧により、強誘電性液晶が前記第1または第2の配向状態、即ち、強誘電性液晶の螺旋構造を解いた状態に設定されるので、その後、書き込み電圧を印加した際、表示階調がほぼ一義的に定まる。従って、階調表示が可能となる。前期選択期間を複数の行で同一タイミングとすることにより、行毎に前期選択期間を設ける場合に比較して、書き込み時間を短くすることができる。初期化電圧を第1と第2のパルス対とし、また、補償電圧を液晶に印加することにより、液晶に印加される電圧の直流成分を除去できる。

【0021】

【実施例】以下、本発明の一実施例を図面を参照して説明する。まず、本発明の駆動方法によって表示駆動される強誘電性液晶表示素子の構成を説明する。図4は強誘電性液晶表示素子の断面図、図5は前記液晶表示素子の画素電極とアクティブ素子を形成した基板の平面図である。

【0022】この強誘電性液晶表示素子は、アクティブマトリクス方式のものであり、一对の透明基板(例えば、ガラス基板)1、2のうち、図4において下側の基

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板（以下、下基板）1には透明な画素電極3と画素電極3に接続されたアクティブ素子4とがマトリクス状に配列形成されている。

【0023】アクティブ素子4は、例えば、薄膜トランジスタ（以下、TFT）から構成される。TFT4は、基板1上に形成されたゲート電極と、ゲート電極を覆うゲート絶縁膜と、ゲート絶縁膜の上に形成された半導体層と、半導体層の上に形成されたソース電極及びドレイン電極とから構成される。

【0024】さらに、下基板1には、図5に示すように、画素電極3の行間にゲートライン（走査ライン）5が配線され、画素電極3の列間にデータライン（階調信号ライン）6が配線されている。各TFT4のゲート電極は対応するゲートライン5に接続され、ドレイン電極は対応するデータライン6に接続されている。

【0025】ゲートライン5は、端部5aを介して行ドライバ（行駆動回路）21に接続され、データライン6は端部6aを介して列ドライバ（列駆動回路）22に接続される。行ドライバ21は、後述するゲートパルスを印加して、ゲートライン5をスキャンする。一方、列ドライバ22は、表示データ（階調データ）を受け、データライン6に表示データに対応するデータ信号を印加する。ゲート信号とデータ信号の詳細は後述する。

【0026】ゲートライン5は端部5aを除いてTFT4のゲート絶縁膜（透明膜）で覆われており、データライン6は前記ゲート絶縁膜の上に形成されている。画素電極3は前記ゲート絶縁膜の上に形成されており、その一端部においてTFT4のソース電極に接続されている。

【0027】図4において、上側の基板（以下、上基板）2には、下基板1の各画素電極3と対向する透明な対向電極7が形成されている。対向電極7は表示領域全体にわたる面積の1枚の電極から構成され、一定の基準電圧V<sub>0</sub>が印加されている。

【0028】下基板1と上基板2の電極形成面には、それぞれ配向膜8、9が設けられている。配向膜8、9はポリイミド等の有機高分子化合物からなる水平配向膜であり、その対向面にはラビングによる配向処理が施されている。

【0029】下基板1と上基板2は、その外周縁部において枠状のシール材10を介して接着されており、基板1、2間のシール材10で囲まれた領域には液晶11が封入されている。液晶11は、カイラルスメクティックC相の螺旋ピッチが両基板1、2の間隔より小さく、かつ、配向状態のメモリ性を有さない強誘電性液晶（以下、DHF液晶）である。このDHF液晶11は、螺旋ピッチが、可視光帯域の波長である700nm～400nm以下（例えば、400nm～300nm）であり、自発分極が大きく、コーンアングルが約27度ないし45°（望ましくは、27°ないし30°）の強誘電性液晶組成物

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からなる。なお、図4において、符号12は両基板1、2の間隔を規制する透明なギャップ材を示し、このギャップ材12は液晶封入領域内に点在状態で配置されている。

【0030】DHF液晶11は、カイラルスメクティックC相が有する層構造の層の法線を配向膜8、9の配向処理の方向に向けて均一な層構造を形成する。また、その螺旋ピッチが基板間隔より小さいため、螺旋構造をもった状態で基板1、2間に封入されている。液晶層を挟んで対向する画素電極3と対向電極7との間に絶対値が所定の値より高い電圧を印加したとき、DHF液晶11は印加電圧の極性に応じて、液晶分子が一方方向に配向する第1の配向状態と液晶分子が他方向に配向する第2の配向状態のいずれかの状態に設定され、また、絶対値が前記所定値より低い電圧を印加画素電極3と対向電極7間に印加したときは、DHF液晶11の螺旋が歪むことにより、液晶分子の平均的な配列状態が、印加電圧に応じて、第1と第2の配向状態の中間の状態となる。

【0031】液晶表示素子の上下には、一対の偏光板13、14が配置されている。偏光板13、14の透過軸の方向は、前述の第1と第2の配向状態におけるDHF液晶11の液晶分子の配向方向に応じて設定されている。

【0032】偏光板13、14の透過軸とDHF液晶11の液晶分子の配向方向との関係を図6を参照して説明する。図6（a）は図4において上側の偏光板（以下、上偏光板）14の透過軸14aを示し、（b）はDHF液晶11の第1と第2の配向状態における液晶分子の配向方向11a、11bを示し、（c）は図4において下側の偏光板（以下、下偏光板）13の透過軸13aを示している。

【0033】一方の極性でかつ絶対値が所定の値以上の電圧を印加した時、DHF液晶11は、第1の配向状態となり、液晶分子は図6（b）に実線で示す第1の配向方向11aに配向する。他方の極性でかつ絶対値が所定の値以上の電圧を印加したとき、DHF液晶11は第2の配向状態となり、液晶分子は図6（b）に波線で示す第2の配向方向に配向する。第1の配向方向11aと第2の配向方向11bとのずれ角θは、DHF液晶11の種類によって異なるが、25°～45°に選定され、望ましくは27°～45°である。

【0034】一対の偏光板13、14のうち、一方の偏光板、例えば、上偏光板14の透過軸14aは、DHF液晶11の2つの配向方向11a、11bの一方、例えば、第2の配向方向11bとほぼ平行になっており、他方の下偏光板13の透過軸13aは、上偏光板14の透過軸14aとほぼ直交している。

【0035】図6に示すように偏光板13、14の透過軸を設定した強誘電性液晶表示素子は、液晶分子を第1の配向方向11aに配向させた時に透過率が最も高く

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(表示が最も明るく) なり、液晶分子を第2の配向方向11bに配向させた時に透過率が最も低く(表示が最も暗く) なる。

【0036】すなわち、液晶分子が第1の配向方向11aを向いた状態では、入射側の偏光板を通過した直線偏光はDHF液晶11の偏光作用により非直線偏光となり、出射側偏光板の透過軸と平行な成分が出射側の偏光板を透過して出射する。このため、表示は明るくなる。一方、液晶分子が第2の配向方向11bを向いた状態では、入射側の偏光板を通った直線偏光はDHF液晶11の偏光作用をほとんど受けず、直線偏光のまま液晶層を通過し、そのほとんどが他方の偏光板で吸収され、表示が暗くなる。

【0037】次に、上記構成の強誘電性液晶表示素子の駆動方法を図1、図2を参照して説明する。図1は、この実施例の液晶表示装置の任意の第K行〜第K+7行( $K=8n+1$ 、 $n$ は0または正の正数)の画素電極3に印加される電圧波形、図2は、第1行〜第16行のゲートライン及び各データラインに印加されるパルス信号の電圧波形を示す。

【0038】本実施例においては、各行の画素(各ゲートライン)の選択期間(書き込み期間)は前期選択期間と後期選択期間から構成され、前期選択期間は複数(8つ)の行で同一タイミングであり、後期選択期間は行毎に異なる。この実施例では、前記選択期間及び後期選択期間をそれぞれ期間 $\Delta t$ (例えば、約45 $\mu$ 秒)のスロットに等分し、後期選択期間の後半のスロットを書き込みパルスP4の印加期間とし、後期選択期間の前半のスロットを書き込みパルスP4に対する補償パルスP3の印加期間とし、前期選択期間の後半のスロットをDHF液晶11を第2の配向状態に設定するためのリセットパルスP2の印加期間とし、前期選択期間の前半のスロットをリセットパルスP2に対する補償パルスP1の印加期間としている。

【0039】まず、図2(a)〜(d)に示すように、第1行〜第8行の画素の前期選択期間に、行ドライバ21は第1行〜第8行のゲートライン5に同時にゲートパルスを印加し、第1行〜第8行のTFT4を同時にオンさせる。この間、コラムドライバ22はすべてのデータライン6に、図2(h)に示すように、正極性の第1リセットパルスP1と負極性の第2リセットパルスP2を印加する。第2リセットパルスP2は液晶表示素子のヒステリシスをなくすために、DHF液晶11を第2の配列状態に設定するためのパルスであり、この第2リセットパルスP2の電圧値 $-VR$ は液晶分子のほとんどの長軸が第2の方向11bに配列するのに十分な値である。また、第1リセットパルスP1は第2リセットパルスP2の印加によりDHF液晶11に直流電圧が片寄ってかかるのを補償するためのパルスであり、第1リセットパルスP1と第2リセットパルスP2の電圧は絶対値が等

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しくて、極性が逆である。

【0040】なお、これら各パルスP1、P2の極性及び電圧値は、いずれも、データ信号の基準電圧V0に対する極性と電圧である。この基準電圧V0は対向電極7に印加する電圧と同一である。また、ゲートライン5に供給されるゲートパルスのパルス幅はデータライン6に供給されるパルス対のパルス幅より狭い。これは、パルス対の後半のパルスの電圧レベルを正確に各画素の容量(画素電極3、対向電極7、DHF液晶11から構成される容量)に保持するためである。図2では、図面を見やすくするため、ゲートパルスとデータライン上のパルス対のパルス幅の差を強調している。

【0041】ゲートパルスがオフすると、トランジスタ4もオフし、第1行〜第8行の各画素の容量は、第2のリセットパルスP2の電圧 $-VR$ にほぼ等しい電圧を保持する。正の電圧で白(光透過)が画素に書き込まれ、負の電圧で黒(光不透過)が画素に書き込まれるとすると、第1行〜第8行の画素はすべて黒の状態(ブランキング)状態となる。

【0042】その後、第1行の画素の後期選択期間が開始し、行ドライバ21は第1行のゲートライン5にゲートパルスを印加し、第1行のゲートライン5に接続されたTFT(第1行のTFT)4がオンする。一方、列ドライバ22は各データラインに、第1行の画素の表示階調に対応する電圧(書き込み電圧)VDを有する書き込みパルスP4と補償パルスP3を印加する。補償パルスP3は書き込みパルスP4の印加によりDHF液晶11に直流電圧が片寄って印加されるのを補償するためのパルスであり、書き込みパルスP4と逆極性で絶対値が同一の電圧を有する。この実施例では、書き込み電圧VDの最小値を電圧V0とし、最大値Vmaxを第2リセットパルスP2の電圧VRより若干低い値とし、V0〜Vmaxの範囲で書き込み電圧を表示階調に応じて制御する。

【0043】書き込みパルスP4がデータライン6に印加されている間に、行ドライバ21はゲートパルスをオフし、第1行のTFT4をオフする。このため、第1行の画素電極3に印加される電圧の波形は図1(a)に示すように、前期選択期間に印加されるリセットパルスP1とP2の対と後期選択期間に印加される補償パルスP3と書き込みパルスP4の対となる。

【0044】第1行の各画素の容量は、第1行のTFT4がオフした際に印加されていた電圧、即ち、書き込みパルスP4の電圧VDにほぼ等しい電圧を保持する。このため、第1行の画素は、次のフレームの前期選択期間まで、書き込み電圧VDに対応する階調、すなわち、表示データに対応する階調を維持する。

【0045】以後、第2、第3、…、第8行のゲートライン5の後期選択期間となり、行ドライバ21は図2(b)〜(d)に示すように、第2、第3、…、第8行のゲートライン5にゲートパルスを順次印加し、列ド



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ライバ22は、図2 (h) に示すように、各データライン6に補償パルスP3と表示データに対応した書き込み電圧VDを有する書き込みパルスP4を印加する。この結果、第2行～第8行の画素電極3には、図1 (b) ～ (h) に示す波形のパルス信号がそれぞれ印加され、第2行～第8行の画素の容量は、第2行～8行のTF T4がオフした際に印加されていた電圧、即ち、書き込みパルスP4の電圧VDにはほぼ等しい電圧を保持し、これにより、表示データに対応する階調を第1行～第8行のゲートラインの次の前期選択期間まで維持する。以上で、第1行～第8行の画素への書き込みが終了する。

【0046】その後、第9行～第16行の画素の前期選択期間になり、行ドライバ21は、図2 (e) ～ (g) に示すように、第9行～第16行のゲートライン5に同時にゲートパルスを印加する。一方、列ドライバ22は、各データライン6に第1リセットパルスP1と第2リセットパルスP2の対を印加する。その後、順次、第9行～第16行の画素の後期選択期間となり、行ドライバ21は、図2 (e) ～ (g) に示すように、第9、第10、…、第16行のゲートライン5にゲートパルスを順次印加し、列ドライバ22は、図2 (h) に示すように、各データライン6に補償パルスP3と書き込みパルスP4を印加する。この結果、第9行～第16行の画素電極3には、図1 (a) ～ (h) に示す波形の電圧パルスが印加され、第9行～第16行の画素は、表示データに対応する階調を第9行～第16行の画素の次の前期選択期間まで維持する。

【0047】以後、同様の動作が8行毎に繰り返され、すべての行の画素への書き込みが終了した時点で書き込み動作は終了する。そして、次のフレームが開始すると、第1行の画素より、再び、上述の動作が繰り返される。

【0048】以上説明した書き込み動作の全体の流れは図3 (a) ～ (d) に示すようになる。なお、図3 (a) と (d) はこの液晶表示素子の一画面分を示し、図3 (b) と (c) は一画面のうちの8行分を示す。

【0049】まず、第1行～第8行の画素にリセットパルス対が印加され、図3 (a) にハッチングを付して示すように、第1行～第8行の画素がすべて黒（ブランク状態）に設定される（第1行～第8行の画素の前期選択期間）。次に、第1行の画素に補償パルスP3と書き込みパルスP4の対が印加され、図3 (b) に示すように、第1行の画素が表示データに対応した階調に設定される（第1行の画素の後期選択期間）。

【0050】次に、第2行の画素に補償パルスP3と書き込みパルスP4の対が印加され、図3 (c) に示すように、第2行の画素が表示データに対応した階調に設定される（第2行の画素の後期選択期間）。以後、同様の動作が第8行の画素まで繰り返され、第1行～第8行の画素が表示データに対応した階調に設定される。

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【0051】その後、第9行～第15行の画素にリセットパルスP1、P2の対が印加され、図3 (d) に示すように、第9行～第15行の画素がすべて黒（ブランク状態）に設定される（第9行～第15行の画素の前期選択期間）。次に、第9行～第15行の画素電極3に補償パルスP3と書き込みパルスP4の対が順次印加され、図3 (b)、(c) に示すように、各行の画素が、順次、表示データに対応した階調に設定される。

【0052】以後、同様の動作が繰り返され、1画面全体に表示データの書き込みが終了すると、再び、図3 (a) に示すように、第1行～第8行の画素にリセットパルスP1、P2の対が印加される。

【0053】上記実施例によれば、複数行の画素を同時にブランキング状態に設定できる。このため、各行の画素の選択期間に個別にリセットパルス対を印加する場合に比較して、一画面分の書き込み時間を短縮することができる。また、列ドライバ22でのデータ処理が容易になり、列ドライバ22の構造を簡略化できる。

【0054】次に、行ドライバ21及び列ドライバ22の構成の一例を図7を参照して説明する。列ドライバ22は例えば、タイミング信号生成回路31、電圧生成回路32、選択信号生成回路33、選択回路34より構成される。例えば、選択信号生成回路33と選択回路34はデータライン毎に配置され、タイミング信号生成回路31と電圧生成回路32は複数のデータライン6に共通に配置される。

【0055】タイミング信号生成回路31は、例えば、周期 $\Delta t$ のクロック信号を生成する。電圧生成回路32は、データライン6に印加する複数の電圧を生成する。選択信号生成回路33には、クロック信号と画素単位の表示データが供給される。第1行、第2行、…の各画素の表示データを、例えば、X1、X2、…、X8、X9、…と仮定すると、選択信号生成回路33は、8画素毎にリセットパルスの電圧VRに対応するデータXRを挿入し、選択データXR、-XR、-X1、X1、-X2、X2、-X3、…、-X8、X8、XR、-XR、-X9、X9、…を生成する。選択回路34は、電圧生成回路32から供給される複数の電圧の内、選択データに対応するものを選択し、データライン6に供給する。

【0056】一方、行ドライバ21は、走査（アドレス）データ生成回路41と走査データ生成回路41の出力データに対応する電圧をゲートライン5に印加するドライバ42から構成される。走査データ生成回路41は、タイミング信号生成回路33から供給されるクロック信号に従って、ゲートパルスに対応するデータ列を生成し、ドライバ42に供給する。

【0057】上記駆動方法により、前述した強誘電性液晶素子の階調制御を行った。この駆動方法においては、パルス幅 $\Delta t$ を $4.5 \mu s$ 、リセットパルスの電圧VRを

(8)

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1.7V、書き込み電圧VDを $0 \leq VD \leq 1.4V$ に設定した。その結果を図8に示す。図8(a)は、図1(a)のように、リセットパルス対と書き込みパルス対を連続して画素に印加した場合の特性、図8(b)は、図1(h)のように、リセットパルス対を印加した後、7選択期間( $7 \cdot 2\Delta t$ )経過後に書き込みパルス対を画素に印加した場合の特性を示す。いずれの場合も、明確な階調表示が可能である。

【0058】なお、前述のように、データライン上の信号レベルを正確に画素電極3、対向電極7、DHF液晶11よりなる容量に保持するためには、データライン上の信号レベルが変化する少し前にゲートパルスがオフすることが望ましい。

【0059】なお、上記実施例では、8つのゲートラインの前期選択期間を同一タイミングにしたが、8つに限定されず、2以上のいずれでもよい。また、複数のゲートラインの前期選択期間を同一タイミングにすることなく、別々のタイミングとしてもよい。この場合も、1つの行の選択期間を前期選択期間と後期選択期間に分け、前期選択期間にリセットパルス対をデータライン6に印加し、後期選択期間に書き込みパルスと補償パルスの対をデータライン6に印加する。

【0060】但し、前期選択期間を共有する行の数が多すぎると、ブランキング状態に設定されてから、最後の行の画素にデータを書き込むまでの時間が長くなりすぎ、表示がちらつくという問題が発生する。また、前期選択期間を共有する行の数が少ないと、個別に前期選択期間が設定されるに等しい状態になり、1画面分の書き込み時間が長くなるという問題がある。実験的には、行数、即ち、ゲートライン5の数が200ないし400程度の場合、前期選択期間を共有する行の数は6ないし10、特に8が望ましい。

【0061】なお、上記実施例では、第1と第2のリセットパルスP1、P2の電圧をVR、-VRとし、この順番でゲートラインに印加しているが、第1と第2のリセットパルスP1、P2の印加の順番は逆でもよい。この場合、各画素は、前期選択期間で白(光透過状態)に設定され、その後、後期選択期間で、表示データに対応する階調に設定される。人間の目の感度が、黒よりも白に敏感であるため、前期選択期間で各画素を黒状態に設定の方が望ましい。

【0062】リセット電圧VR、-VRは、DHF液晶11の液晶分子の長軸(ダイレクタ)がほとんど第1または第2の配向方向11a、11bに配向する電圧であればよく、配向方向11a、11bに完全に配向する電圧でなくてもよい。

【0063】上記実施例では、前期選択期間に、第1リセットパルスと第2リセットパルスを1回づつ画素に印加しているが、第1リセットパルスと第2リセットパルスの印加回数が同じならば、印加回数は任意でよい。

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【0064】上記実施例で駆動した強誘電性液晶表示素子は、一方の偏光板14の透過軸14aをDHF液晶11の第2の配向方向11bとほぼ平行にしたものであるが、上記駆動方法は、一方の偏光板14の透過軸14aをDHF液晶11の第1の配向方向11aとほぼ平行にした、DHF液晶11を第2の配向方向11bに配向させた際に透過率が最も高く(表示が最も明るく)なり、DHF液晶11を第1の配向方向11aに配向させたときに透過率が最も低く(表示が最も暗く)なる強誘電性液晶表示素子の駆動にも適用できる。また、本発明の駆動方法はTFTをアクティブ素子とする強誘電性液晶表示素子に限らず、MIMをアクティブ素子とする強誘電性液晶表示素子にも適用可能である。

【0065】

【発明の効果】以上説明したように、本発明の液晶表示装置及び液晶表示素子の駆動方法によれば、前期選択期間に液晶を第1の配向状態に配向させる電圧と第2の配向状態に配向させる電圧の少なくとも一方を画素に印加して、液晶分子を一定の配向状態とし、その後、後期選択期間に表示データに対応する書き込み電圧を画素に印加する。従って、基板間隔より小さい螺旋ピッチを持った非メモリ性強誘電性液晶(DHF液晶)を用いたアクティブマトリクス方式の強誘電性液晶表示素子に、明確な階調表示を行なわせることができる。また、複数のゲートラインの前期選択期間を共通にすることにより、1フィールドの書き込み時間を短くすることができる。

【図面の簡単な説明】

【図1】(a)～(h)は、この発明の一実施例にかかる液晶表示素子の駆動方法により、第K行～第K+7行の画素に印加される電圧の波形を示すタイミングチャートである。

【図2】(a)～(g)は、この発明の一実施例にかかる液晶表示素子の駆動方法により、第1行～第16行のゲートラインに印加される電圧の波形を示すタイミングチャート、(h)は、データラインに印加される電圧の波形を示すタイミングチャートである。

【図3】本実施例による書き込み手順を示す図であり、(a)と(d)は一画面を示す図、(b)と(c)は8行分の画素を示す図である。

【図4】この発明の一実施例にかかる液晶表示素子の駆動方法により駆動される液晶表示素子の構造を示す断面図である。

【図5】図4に示す液晶表示素子の下基板の構成を示す平面図である。

【図6】偏光板の透過軸と液晶分子の配向方向の関係を示す図であり、(a)は上基板の透過軸の方向、(b)は液晶分子の配向方向、(c)は下基板の透過軸の方向をそれぞれ示す図である。

【図7】行ドライバ及び列ドライバの構成の一例を示すブロック図である。



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【図8】印加電圧と透過率の変化を示すグラフである。

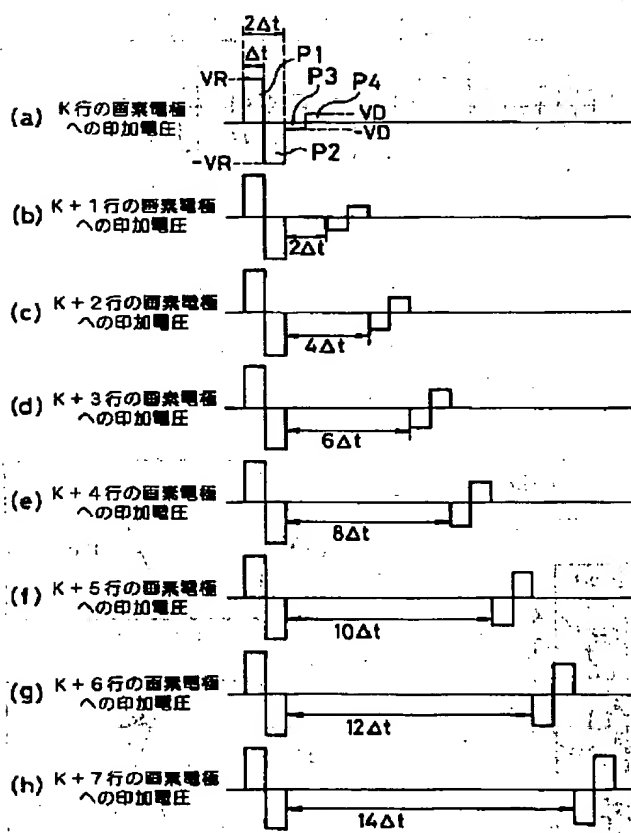
【符号の説明】

- 1 透明基板（下基板）
- 2 透明基板（上基板）
- 3 画素電極
- 4 アクティブ素子（TFT）
- 5 ゲートライン（走査ライン）
- 6 データライン（階調信号ライン）
- 7 対向電極
- 8 配向膜
- 9 配向膜
- 10 シール材

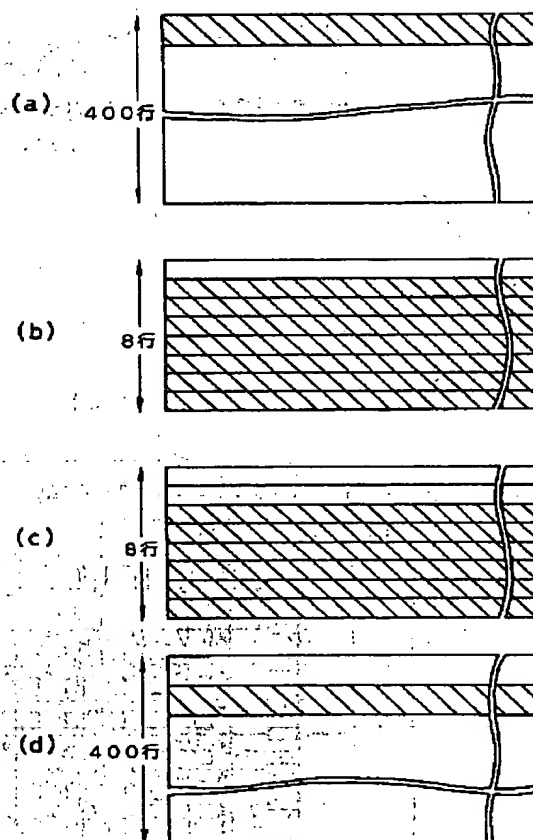
16

- 11 強誘電性液晶（DHF液晶）
- 12 ギャップ材
- 13 偏光板（下偏光板）
- 14 偏光板（上偏光板）
- 21 行ドライバ（行駆動回路）
- 22 列ドライバ（列駆動回路）
- 31 タイミング信号生成回路
- 32 電圧生成回路
- 33 選択信号生成回路
- 34 選択回路34
- 41 走査データ生成回路
- 42 ドライバ

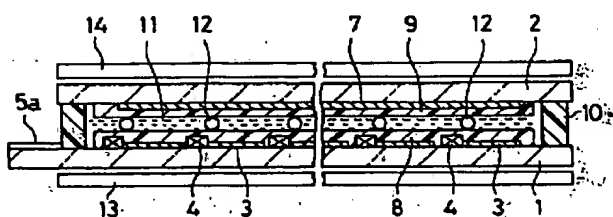
【図1】



【図3】

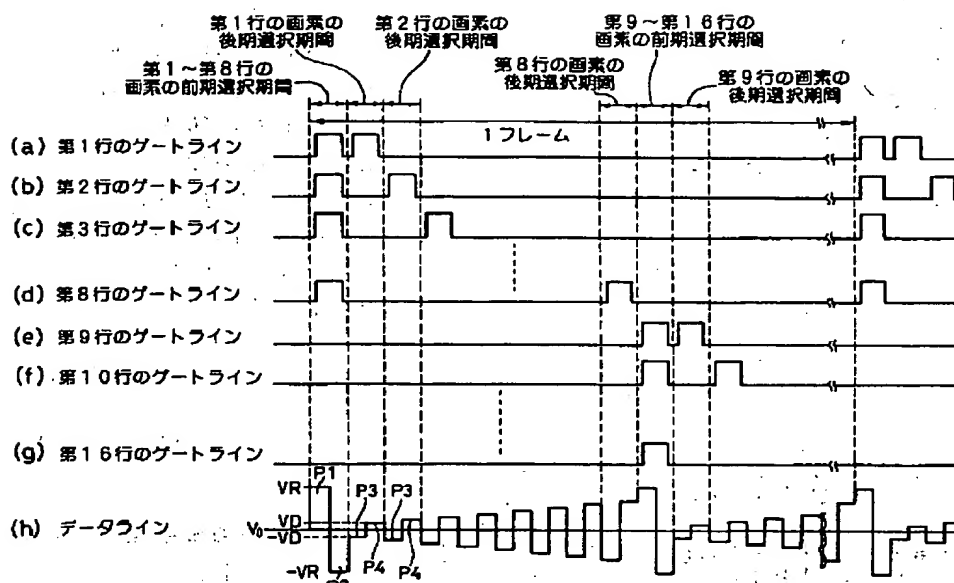


【図4】

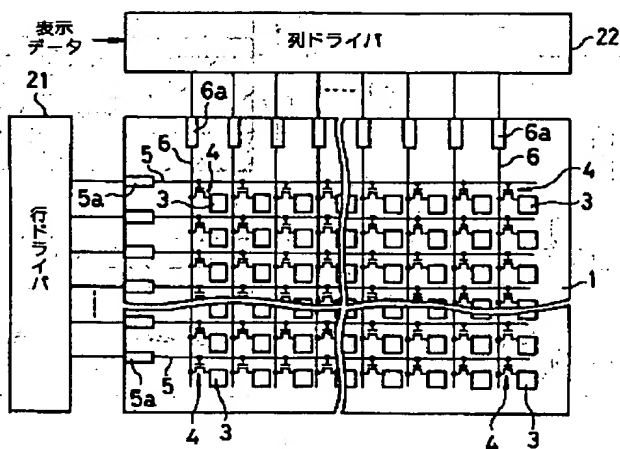


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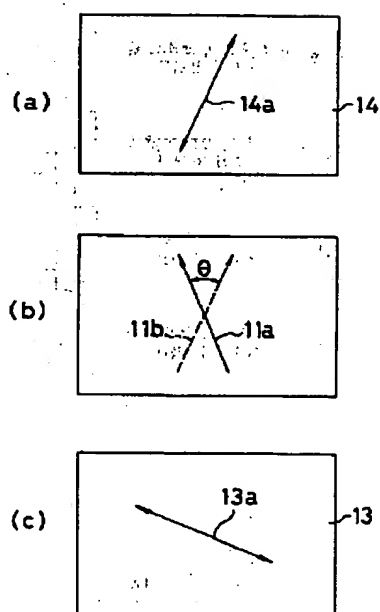
【図2】



【図5】

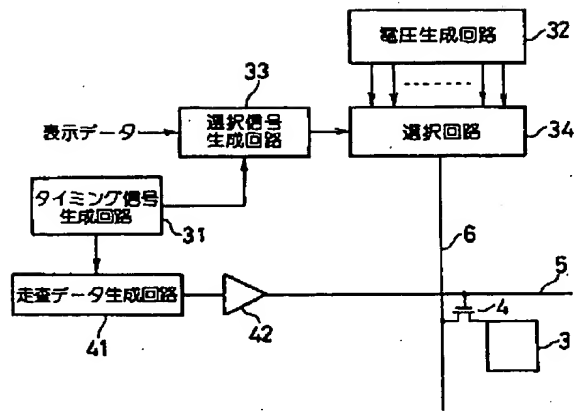


【図6】

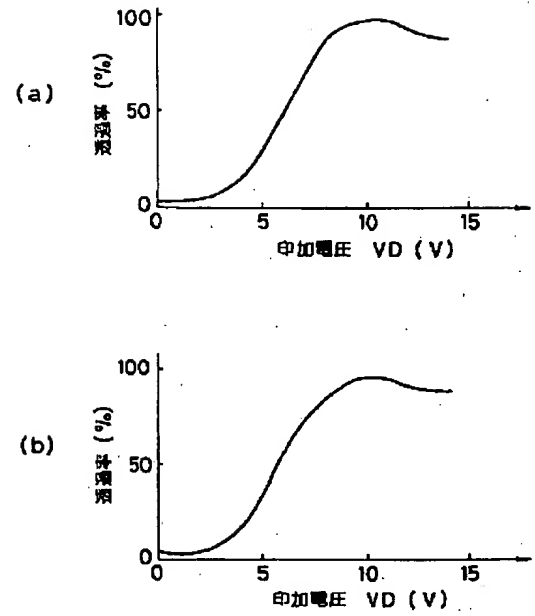


(11)

【図 7】



【図 8】



# PATENT ABSTRACTS OF JAPAN

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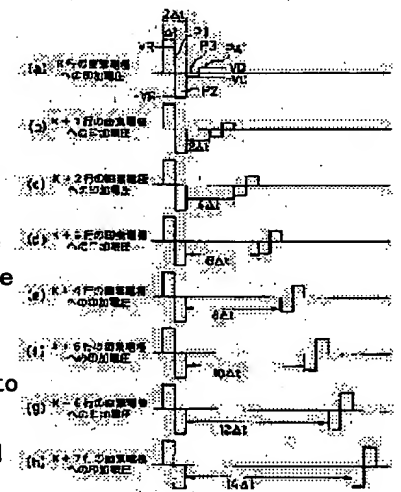
(72)Inventor : TANAKA TOMIO

## (54) FERROELECTRIC LIQUID CRYSTAL DISPLAY DEVICE AND METHOD FOR DRIVING FERROELECTRIC LIQUID CRYSTAL DISPLAY ELEMENT

### (57)Abstract:

**PURPOSE:** To enable an active matrix type ferroelectric liquid crystal display element using a DHF(deformed helix ferroelectric) liquid crystal to perform a clear gradation display and to shorten a writing time.

**CONSTITUTION:** A selection period of a pixel of every row is divided into the first term selection period and the latter term selection period. In the first term selection period, a voltage  $-VR$  sufficient for unbinding the helical structure of the DHF liquid crystal and the voltage  $VR$  having a polarity opposite to and an absolute value equal to the voltage  $-VR$  is applied to the liquid crystal in the prescribed order, and the display element is set to a blanking state. In the latter term selection period, a compensation voltage  $-VD$  and a write voltage  $VD$  are applied to the liquid crystal successively, and the gradation of the pixel is set to the display gradation. The write voltage  $VD$  is changed according to the display gradation, and the compensation pulse is a voltage having the polarity opposite to and the absolute value equal to the write voltage  $VD$ . The first term selection period is set to the pixels of plural rows at the same timing, and the latter term selection period is set at the timing different from each other for every row.



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[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

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**CLAIMS**

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[Claim(s)]

[Claim 1] The substrate with which two or more arrays of the thin film transistor connected to the pixel electrode and the pixel electrode were being carried out steadily at the shape of a matrix, It is arranged between the substrates of another side in which the counterelectrode which counters said pixel electrode was formed, and these substrates. The 1st orientation condition which the liquid crystal molecule arranged mostly in one direction according to the electrical potential difference which had a layer system and the spiral structure of a spiral pitch smaller than spacing of said substrate, and was impressed between said pixel electrodes and counterelectrodes, The non-memory nature ferroelectric liquid crystal which changes orientation into the 2nd orientation condition in which the liquid crystal molecule carried out the \*\*\*\* array in the direction of another side, and the middle orientation condition that the average array direction of a liquid crystal molecule becomes between one [ said ] direction and the directions of another side by distortion of said spiral structure, respectively, The selection period of each pixel which consists of said pixel electrode and counterelectrode, and said ferroelectric liquid crystal inserted into them in the actuation approach of a preparation \*\*\*\*\* display device A selection period is made into the same timing in two or more lines of said matrix said first half in the first half including a selection period and an anaphase selection period. The initialization electrical potential difference which sets said liquid crystal as said 1st orientation condition and one [ at least ] condition of the 2nd orientation condition is impressed between said pixel electrodes and said counterelectrodes. At said anaphase selection period The actuation approach of the ferroelectric liquid crystal display device which considers as different timing for every line of said matrix, and is characterized by what the write-in electrical potential difference which changes according to display gradation is impressed for between said pixel electrodes and said counterelectrodes.

[Claim 2] Said initialization electrical potential difference is the actuation approach according to claim 1 characterized by what the 1st pulse which changes the orientation of said ferroelectric liquid crystal into the 1st orientation condition, and the 2nd pulse which changes the orientation of said ferroelectric liquid crystal into the 2nd orientation condition are included for.

[Claim 3] Said the 1st and 2nd pulse are the actuation approach according to claim 2 that a polarity is characterized by being opposite and an absolute value having an equal electrical potential difference.

[Claim 4] Claim 1 characterized by impressing said write-in electrical potential difference, and said write-in electrical potential difference and a compensation electrical potential difference with an equal absolute value with a reverse and polarity between said pixel electrodes and said counterelectrodes at said anaphase selection period thru/or the actuation approach of any one publication of three.

[Claim 5] Said initialization electrical potential difference is claim 1 characterized by being the electrical potential difference which sets the display of said liquid crystal display component as a black condition thru/or the actuation approach of any one publication of four.

[Claim 6] The substrate with which the active component connected to the pixel electrode and this pixel electrode was being steadily arranged in the shape of a matrix, It is arranged between the substrate of another side in which the counterelectrode which counters said pixel electrode was formed, and said substrate. The 1st orientation condition which the liquid crystal molecule arranged mostly in one direction according to the electrical potential difference which had a layer system and the spiral structure of a spiral pitch smaller than spacing of said substrate, and was impressed between said pixel electrodes and said counterelectrodes, The ferroelectric liquid crystal display device to which the liquid crystal molecule equipped the orientation condition of the middle arbitration of the 2nd orientation condition which carried out the \*\*\*\* array, and said 1st and 2nd orientation condition with the non-memory nature ferroelectric liquid crystal which carries out orientation in the direction of another side, It connects with said active component and said pixel electrode is chosen in the anaphase selection period of timing different a selection period and said first half from a selection period in the first half. Said first half at a selection period The electrical potential difference for setting said ferroelectric liquid crystal as one side

of said 1st or 2nd orientation condition is impressed to said pixel electrode of the multi-line of said matrix through said active component. The ferroelectric liquid crystal display characterized by equipping an anaphase selection period with the driving means which impresses the electrical potential difference which changes according to the display gradation of a pixel to said pixel electrode through said active component.

[Claim 7] Said active component consists of thin film transistors connected to the pixel electrode with which the end of a current path corresponds. Said driving means The gate line connected to the gate of two or more of said thin film transistors of a corresponding line, The data line connected to the other end of the current path of two or more of said thin film transistors of a corresponding train, The line driving means which supplies the gate voltage which makes said thin film transistor turn on to said gate line of the line said first half at a selection period and said anaphase selection period, The initialization electrical potential difference for setting said ferroelectric liquid crystal as one side of said 1st or 2nd orientation condition at a selection period is impressed to said data line said first half. The ferroelectric liquid crystal display according to claim 6 characterized by what said anaphase selection period is equipped with the train driving means corresponding to said display gradation which writes in and impresses an electrical potential difference to said data line for.

[Claim 8] It is the ferroelectric liquid crystal display according to claim 7 which impresses said line driving means to said gate line at said anaphase selection period to timing which is different in said gate voltage in said anaphase selection period by said line driving means's impressing gate voltage to said two or more gate lines simultaneously at a selection period, and said train driving means impressing said initialization electrical potential difference to said data line, and is characterized by what said train driving means impresses said write-in electrical potential difference to said data line for said first half.

[Claim 9] Said train driving means is a ferroelectric liquid crystal display according to claim 7 or 8 characterized by what the 1st pulse which sets said ferroelectric liquid crystal as the 1st orientation condition, and the 2nd pulse which sets said ferroelectric liquid crystal as the 2nd orientation condition are impressed to said data line for in a selection period said first half.

[Claim 10] Said the 1st pulse and 2nd pulse are a ferroelectric liquid crystal display according to claim 9 with which a polarity is characterized by being opposite and an absolute value having an equal electrical potential difference.

[Claim 11] Said train driving means is claim 7 to which it is said write-in electrical potential difference and reversed polarity, and an absolute value is characterized by what an equal compensation electrical potential difference is impressed to said data line for with said write-in electrical potential difference at said anaphase selection period thru/or the ferroelectric liquid crystal display of any one publication of ten.

[Claim 12] Said driving means is claim 6 characterized by setting said ferroelectric liquid crystal display device as a dark condition in a selection period said first half thru/or the ferroelectric liquid crystal display of any one publication of 11.

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[Translation done.]

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#### DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the actuation approach of the short DHF liquid crystal display of write-in time amount in which a gradation display is possible, and a DHF liquid crystal display component especially about the actuation approach of the liquid crystal display using the DHF (Deformed Helix Ferroelectric)



liquid crystal which is a kind of a ferroelectric liquid crystal, and a liquid crystal display component.

[0002]

[Description of the Prior Art] The ferroelectric liquid crystal display device using a ferroelectric liquid crystal attracts attention in respect of a high-speed response and a large angle of visibility being obtained etc. as compared with the liquid crystal display component in TN mode in which a pneumatic liquid crystal is used.

[0003] Research on utilization of this ferroelectric liquid crystal display device was conventionally done for the ferroelectric liquid crystal with which the spiral pitch of the chiral smectic C phase called SS-F liquid crystal has the memory nature (bistability nature) of an orientation condition more greatly than substrate spacing (cell gap) of a liquid crystal device.

[0004] The ferroelectric liquid crystal display device using the above-mentioned SS-F liquid crystal It is what enclosed SS-F liquid crystal between substrates where the spiral structure is vanished. Two orientation conditions with the 2nd orientation condition when impressing the 1st orientation condition when impressing the electrical potential difference of one electrode and the polar electrical potential difference of another side by the interaction of applied voltage and the spontaneous polarization of liquid crystal are acquired. The permeability of light is controlled by the polarizing plate of the couple arranged to the orientation condition [ of this liquid crystal ], incidence [ of a component ], and outgoing radiation side, and it displays.

[0005] However, it is made difficult to make the display in which the ferroelectric liquid crystal display device using the above-mentioned SS-F liquid crystal changes permeability, and gradation is shown since the orientation condition of liquid crystal is in two conditions of the 1st orientation condition and the 2nd orientation condition and one of orientation conditions is maintained also in the state of no electrical-potential-difference impressing perform.

[0006] so, recently, development of the possible ferroelectric liquid crystal display device of a gradation display inquires — having — \*\*\*\* — "LIQUID CRYSTALS", 1989, Vol.5, and NO.4, Using the ferroelectric liquid crystal with which the spiral pitch of a chiral smectic C phase does not have the memory nature of an orientation condition smaller than substrate spacing of a display device is proposed as indicated by the 1171st page thru/or the 1177th page. This ferroelectric liquid crystal is called DHF liquid crystal in distinction from the above-mentioned SS-F liquid crystal.

[0007] After DHF liquid crystal has had spiral structure, it is enclosed between substrates by the ferroelectric liquid crystal display device using DHF liquid crystal. It responds to the electrical potential difference impressed to inter-electrode [ which counters on both sides of a liquid crystal layer ]. DHF liquid crystal The 1st orientation condition which the direction of a major axis of a liquid crystal molecule (director) arranged mostly in the 1st direction, the 2nd orientation condition in which the direction of a major axis of a liquid crystal molecule carried out orientation in the 2nd direction mostly, Or it is set as the medium orientation condition that the average array of the direction of a major axis of a liquid crystal molecule serves as said 1st [ the- ] and the direction of the arbitration between the 2nd direction.

[0008] Unlike the above-mentioned SS-F liquid crystal, the memory nature of an orientation condition does not have DHF liquid crystal, but since it can take a medium orientation condition, if during a non-selection period maintains a medium orientation condition, a gradation display is possible for it.

[0009] As the actuation approach of making a gradation display performing to this ferroelectric liquid crystal display device, how to impress the electrical potential difference (write-in electrical potential difference) according to the gradation which should be displayed on the selection period (write-in period) of each pixel to each pixel is considered conventionally.

[0010] However, by the above-mentioned actuation approach, a write-in electrical potential difference and the transmission of a pixel did not correspond, and control of gradation was impossible and was hardly able to realize the gradation display of practical use level. Even if the optical property (relation between applied voltage and permeability) of DHF liquid crystal has a large hysteresis and this generally impresses the electrical potential difference corresponding to display gradation to DHF liquid crystal simply, it is relation with the electrical potential difference impressed before it, and is for gradation not to become settled uniquely.

[0011] In order to solve such a problem, the initialization electrical potential difference for once setting DHF liquid crystal as one side of the 1st orientation condition and the 2nd orientation condition for every selection period is impressed to DHF liquid crystal, and the actuation approach according to an indicative data which writes in and impresses an electrical potential difference is indicated after that by Japanese Patent Application No. 4-327002.

[0012] By this actuation approach, four pulses are impressed to a pixel electrode at the selection period of the pixel of each line. That is, an active component is turned on, when an absolute value carries out sequential

impression of the 1st [ same ] and the 2nd same reset pulse, and the write-in pulse which has an electrical potential difference corresponding to display gradation and the write-in pulse is impressed, although a compensation pulse with the same absolute value of an electrical-potential-difference value differs from a polarity with a write-in pulse and reversed polarity.

[0013] According to such a configuration, spiral structure is set as a solution beam condition for DHF liquid crystal by the 1st and the 2nd reset pulse, and the electrical potential difference of a write-in pulse is held after that during a non-selection period at each pixel. Therefore, while the gradation corresponding to a write-in electrical potential difference becomes settled uniquely, the gradation is maintained for one frame and the gradation display of it is attained. Moreover, since the 1st, the 2nd reset pulse and a write-in pulse, and a compensation pulse are offset, respectively, a dc component is not generated on the electrical potential difference impressed to DHF liquid crystal.

[0014]

[Problem(s) to be Solved by the Invention] As mentioned above, by the actuation approach of the conventional DHF liquid crystal device, display gradation did not become settled uniquely but there was a problem that a gradation display could not be performed, substantially. Moreover, by the actuation approach indicated by Japanese Patent Application No. 4-327002, in order to make it applied voltage not contain a dc component, it writes in with a reset pulse and, in addition to a pulse, two amendment pulses are needed. For this reason, the data which reversed the bit from the same content at each selection period needed to be transmitted twice to the driver, and the configuration of a display control and a driver was complicated. Moreover, there was also a problem that it was necessary to impress four pulses to a data line for every selection period, and a selection period became long, consequently the write-in period for one screen became long.

[0015] This invention was made in view of the above-mentioned actual condition, and the configuration of a display-control system is comparatively easy, and it aims to let it offer the gradation method of presentation and the DHF liquid crystal display of a DHF liquid crystal display component which enable shortening of the write-in time amount of one screen. Moreover, this invention can make a clear gradation display perform to the ferroelectric liquid crystal display device of an active matrix using the non-memory nature ferroelectric liquid crystal (DHF) liquid crystal which has a spiral pitch smaller than substrate spacing, and changes orientation into the 1st orientation condition, the 2nd orientation condition, and the orientation condition of middle arbitration according to the electrical potential difference to impress, respectively, and aims at moreover offer the actuation approach of the short liquid crystal display component of write-in time amount, and a liquid crystal display to it.

[0016]

[Means for Solving the Problem] In order to attain the above-mentioned object, the actuation approach of the ferroelectric liquid crystal display device concerning this invention The substrate with which two or more arrays of the thin film transistor connected to the pixel electrode and the pixel electrode were being carried out steadily at the shape of a matrix, It is arranged between the substrates of another side in which the counterelectrode which counters said pixel electrode was formed, and these substrates. The 1st orientation condition which the liquid crystal molecule arranged mostly in one direction according to the electrical potential difference which had a layer system and the spiral structure of a spiral pitch smaller than spacing of said substrate, and was impressed between said pixel electrodes and counterelectrodes, The non-memory nature ferroelectric liquid crystal which changes orientation into the 2nd orientation condition in which the liquid crystal molecule carried out the \*\*\*\* array in the direction of another side, and the middle orientation condition that the average array direction of a liquid crystal molecule becomes between one [ said ] direction and the directions of another side by distortion of said spiral structure, respectively, The selection period of each pixel which consists of said pixel electrode and counterelectrode, and said ferroelectric liquid crystal inserted into them in the actuation approach of a preparation \*\*\*\*\* display device A selection period is made into the same timing in two or more lines of said matrix said first half in the first half including a selection period and an anaphase selection period. The initialization electrical potential difference which sets said liquid crystal as said 1st orientation condition and one [ at least ] condition of the 2nd orientation condition is impressed between said pixel electrodes and said counterelectrodes. At said anaphase selection period It considers as different timing for every line of said matrix, and is characterized by what the write-in electrical potential difference which changes according to display gradation is impressed for between said pixel electrodes and said counterelectrodes.

[0017] In order to attain the above-mentioned object, the ferroelectric liquid crystal display concerning this invention The substrate with which the active component connected to the pixel electrode and this pixel electrode was being steadily arranged in the shape of a matrix, It is arranged between the substrate of another

side in which the counterelectrode which counters said pixel electrode was formed, and said substrate. The 1st orientation condition which the liquid crystal molecule arranged mostly in one direction according to the electrical potential difference which had a layer system and the spiral structure of a spiral pitch smaller than spacing of said substrate, and was impressed between said pixel electrodes and said counterelectrodes, The ferroelectric liquid crystal display device to which the liquid crystal molecule equipped the orientation condition of the middle arbitration of the 2nd orientation condition which carried out the \*\*\*\* array, and said 1st and 2nd orientation condition with the non-memory nature ferroelectric liquid crystal which carries out orientation in the direction of another side, It connects with said active component and said pixel electrode, is chosen in the anaphase selection period of timing different a selection period and said first half from a selection period in the first half. Said first half at a selection period The electrical potential difference for setting said ferroelectric liquid crystal as one side of said 1st or 2nd orientation condition is impressed to said pixel electrode of the multi-line of said matrix through said active component. It is characterized by having the driving means which impresses the electrical potential difference which changes according to the display gradation of a pixel to said pixel electrode through said active component at an anaphase selection period.

[0018] In the above-mentioned configuration, the absolute value of the electrical potential difference of said the 1st and 2nd pulse is equal including the 1st pulse by which an initialization electrical potential difference sets liquid crystal as the 1st orientation condition, and the 2nd pulse set as the 2nd orientation condition.

[0019] You may make it impress a write-in electrical potential difference and a compensation electrical potential difference with an equal absolute value with a reverse and polarity to said liquid crystal at an anaphase selection period. An active component consists of thin film transistors. A driving means Moreover, for example, the line driving means which supplies the signal which makes said thin film transistor turn on in said first half of a corresponding line to said gate line corresponding to a selection period and said anaphase selection period, The initialization electrical potential difference for setting said liquid crystal molecule as one side of said 1st or 2nd orientation condition is impressed to a pixel electrode through a thin film transistor in the first half at a selection period. the train driving means corresponding to said display gradation to an anaphase selection period which writes in and impresses an electrical potential difference to a pixel electrode through a thin film transistor — since — it is constituted.

[0020]

[Function] Since a ferroelectric liquid crystal is set with an initialization electrical potential difference to said the 1st or 2nd orientation condition, i.e., the condition of having dispelled the spiral structure of a ferroelectric liquid crystal, according to the above-mentioned configuration, when a write-in electrical potential difference is impressed after that, display gradation becomes settled almost uniquely. Therefore, a gradation display is attained. By making a selection period into the same timing in two or more lines in the first half, write-in time amount can be shortened as compared with the case where a selection period is prepared for every line in the first half. The dc component of the electrical potential difference impressed to liquid crystal is removable by making an initialization electrical potential difference into the 1st and 2nd pulse pair, and impressing a compensation electrical potential difference to liquid crystal.

[0021]

[Example] Hereafter, one example of this invention is explained with reference to a drawing. First, the configuration of a ferroelectric liquid crystal display device by which display actuation is carried out by the actuation approach of this invention is explained. It is the top view of a substrate in which drawing 4 formed the sectional view of a ferroelectric liquid crystal display device in, and drawing 5 formed the pixel electrode of said liquid crystal display component, and the active component.

[0022] This ferroelectric liquid crystal display device is the thing of an active matrix, and array formation of the active component 4-connected to the lower pixel electrode 3 transparent to a substrate (henceforth, bottom-substrate) 1 and the lower pixel electrode 3 in drawing 4 among the transparence substrates (for example, glass substrate) 1 and 2 of a couple is carried out at the shape of a matrix.

[0023] The active component 4 consists of thin film transistors (following, TFT). TFT4 consists of the source electrodes and drain electrodes which were formed in the gate electrode formed on the substrate 1, and the gate electrode on wrap gate dielectric film, the semi-conductor layer formed on gate dielectric film, and the semi-conductor layer.

[0024] Furthermore, as shown in the bottom substrate 1 at drawing 5, the gate line (scan line) 5 is wired by the space of the pixel electrode 3, and the data line (gradation signal line) 6 is wired between the trains of the pixel electrode 3. The gate electrode of each FTF4 is connected to the corresponding gate line 5, and the drain

electrode is connected to the corresponding data line 6.

[0025] The gate line 5 is connected to the line driver (line actuation circuit) 21 through edge 5a, and a data line 6 is connected to the train driver (train actuation circuit) 22 through edge 6a. The line driver 21 impresses the gate pulse mentioned later, and scans the gate line 5. On the other hand, the train driver 22 receives an indicative data (gradation data), and impresses the data signal corresponding to an indicative data to a data line 6. The detail of a gate signal and a data signal is mentioned later.

[0026] The gate line 5 is covered with the gate dielectric film (transparent membrane) of TFT4 except for terminal area 5a, and the data line 6 is formed on said gate dielectric film. The pixel electrode 3 is formed on said gate dielectric film, and is connected to the source electrode of TFT4 in the end section.

[0027] In drawing 4, each pixel electrode 3 of the bottom substrate 1 and the transparent counterelectrode 7 which counters are formed in the upper substrate (henceforth, top substrate) 2. A counterelectrode 7 consists of electrodes of one sheet of the area covering the whole viewing area, and the fixed reference voltage  $V_0$  is impressed.

[0028] The orientation film 8 and 9 is formed in the electrode forming face of the bottom substrate 1 and the top substrate 2, respectively. The orientation film 8 and 9 is level orientation film which consists of organic high molecular compounds, such as polyimide, and orientation processing by rubbing is performed to the opposed face.

[0029] The bottom substrate 1 and the top substrate 2 are pasted up through the frame-like sealant 10 at the periphery edge, and liquid crystal 11 is enclosed with the substrate 1 and the field surrounded by the sealant 10 between two. Liquid crystal 11 has the spiral pitch of a chiral smectic C phase smaller than spacing of both the substrates 1 and 2, and it is the ferroelectric liquid crystal (henceforth, DHF liquid crystal) which does not have the memory nature of an orientation condition. A spiral pitch is 700nm – 400nm or less (for example, 400nm – 300nm) which is the wavelength of a light band, this DHF liquid crystal 11 has large spontaneous polarization, and a cone angle type consists of a ferroelectric liquid crystal constituent (about 27 degrees thru/or 45 degrees (desirably 27 degrees thru/or 30 degrees)). In addition, in drawing 4, a sign 12 shows the transparent gap material which regulates spacing of both the substrates 1 and 2, and this gap material 12 is arranged in the state of scattering in the liquid crystal enclosure field.

[0030] The DHF liquid crystal 11 turns the normal of the layer of the layer system which a chiral smectic C phase has towards the orientation film 8 and orientation processing of nine, and forms a uniform layer system. Moreover, since the spiral pitch is smaller than substrate spacing, where it has spiral structure, it is enclosed between a substrate 1 and 2. When an electrical potential difference with an absolute value higher than a predetermined value is impressed between the pixel electrodes 3 and counterelectrodes 7 which counter on both sides of a liquid crystal layer, The DHF liquid crystal 11 is set as one condition of the 2nd orientation condition in which the 1st orientation condition and liquid crystal molecule in which a liquid crystal molecule carries out orientation to an one direction carry out orientation in the other directions according to the polarity of applied voltage. Moreover, when an electrical potential difference with an absolute value lower than said predetermined value is impressed between the impression pixel electrode 3 and a counterelectrode 7, and the spiral of the DHF liquid crystal 11 is distorted, the average array condition of a liquid crystal molecule will be in the 1st and the middle condition of the 2nd orientation condition according to applied voltage.

[0031] The polarizing plates 13 and 14 of a couple are arranged at the upper and lower sides of a liquid crystal display component. The transparency shaft orientation of polarizing plates 13 and 14 is set up according to the direction of orientation of the liquid crystal molecule of the DHF liquid crystal 11 in the above-mentioned 1st and 2nd orientation condition.

[0032] The relation between the transparency shaft of polarizing plates 13 and 14 and the direction of orientation of the liquid crystal molecule of the DHF liquid crystal 11 is explained with reference to drawing 6. Drawing 6 (a) shows transparency shaft 14a of the upper polarizing plate (henceforth, top polarizing plate) 14 in drawing 4, (b) shows the directions 11a and 11b of orientation of the liquid crystal molecule in the 1st [ of the DHF liquid crystal 11 ], and 2nd orientation condition, and (c) shows transparency shaft 13a of the lower polarizing plate (henceforth, bottom polarizing plate) 13 in drawing 4.

[0033] It is one polarity, and when the electrical potential difference beyond a value predetermined in an absolute value is impressed, the DHF liquid crystal 11 will be in the 1st orientation condition, and will carry out orientation of the liquid crystal molecule to 1st direction of orientation 11a shown in drawing 6 (b) as a continuous line. It is the polarity of another side, and when the electrical potential difference beyond a value predetermined in an absolute value is impressed, the DHF liquid crystal 11 will be in the 2nd orientation condition, and will carry out orientation of the liquid crystal molecule in the 2nd direction of orientation shown in drawing 6 (b) with a wavy line.

Although the gap angle  $\theta$  of 1st direction of orientation 11a and 2nd direction of orientation 11b changes with classes of DHF liquid crystal 11, it is selected by 25 degrees – 45 degrees, and is 27 degrees – 45 degrees desirably.

[0034] transparency shaft 14a of one [ among the polarizing plates 13 and 14 of a couple ] polarizing plate 14, for example, a top polarizing plate; — the two directions 11a and 11b of orientation of the DHF liquid crystal 11 — on the other hand, it is parallel mostly with 2nd direction of orientation 11b, and transparency shaft 13a of the bottom polarizing plate 13 of another side lies at right angles to transparency shaft 14a of the top polarizing plate 14 mostly.

[0035] the time of the ferroelectric liquid crystal display device which set up the transparency shaft of polarizing plates 13 and 14 as shown in drawing 6 carrying out orientation of the liquid crystal molecule to 1st direction of orientation 11a — permeability — most — being high (a display the brightest) — when carrying out orientation of the liquid crystal molecule to 2nd direction of orientation 11b, permeability becomes the lowest (a display most darkly).

[0036] That is, after the liquid crystal molecule has turned to 1st direction of orientation 11a, the linearly polarized light which passed the polarizing plate by the side of incidence turns into nonlinear polarization by the polarization of the DHF liquid crystal 11, and a component parallel to the transparency shaft of an outgoing radiation side polarizing plate penetrates the polarizing plate by the side of outgoing radiation, and it carries out outgoing radiation. For this reason, a display becomes bright. On the other hand, after the liquid crystal molecule has turned to 2nd direction of orientation 11b, the linearly polarized light which passed along the polarizing plate by the side of incidence hardly receives the polarization of the DHF liquid crystal 11, but a liquid crystal layer is passed with the linearly polarized light, the most is absorbed with the polarizing plate of another side, and a display becomes dark.

[0037] Next, the actuation approach of the ferroelectric liquid crystal display device of the above-mentioned configuration is explained with reference to drawing 1 and drawing 2. The voltage waveform by which drawing 1 is impressed to the pixel electrode 3 of — of Kth line the K+7th line ( $K=8n+1$  and  $n$  are 0 or a forward positive number) of the arbitration of the liquid crystal display of this example, and drawing 2 show the voltage waveform of the pulse signal impressed to the gate line of — of 1st line the 16th line, and each data line.

[0038] In this example, the selection period (write-in period) of the pixel (each gate line) of each line consists of a selection period and an anaphase selection period in the first half, a selection period is the same timing in the line of plurality (eight) in the first half, and anaphase selection periods differ for every line. In this example, said selection period and an anaphase selection period, respectively Period.deltat Divide equally into the slot for (for example, about 45 microseconds), write in the slot in the second half of an anaphase selection period, and it considers as the impression period of a pulse P4. Write in the slot in the first half of an anaphase selection period, and it considers as the impression period of the compensation pulse P3 over a pulse P4. The slot in the second half of a selection period is made into the impression period of the reset pulse P2 for setting the DHF liquid crystal 11 as the 2nd orientation condition, and is made into the impression period of the compensation pulse [ as opposed to a reset pulse P2 for the slot in the first half of a selection period ] P1 in the first half in the first half.

[0039] First, the line driver 21 impresses a gate pulse to the gate line 5 of — of 1st line the 8th line simultaneously, and makes the first half selection period of the pixel of — of 1st line the 8th line turn on simultaneously TFT4 of — of 1st line the 8th line, as shown in drawing 2 (a)–(d). In the meantime, the column driver 22 impresses the 1st reset pulse P1 of straight polarity, and the 2nd reset pulse P2 of negative polarity to all the data lines 6, as shown in drawing 2 (h). In order that the 2nd reset pulse P2 may abolish the hysteresis of a liquid crystal display component, it is a pulse for setting the DHF liquid crystal 11 as the 2nd array condition; and electrical-potential-difference value-VR of this 2nd reset pulse P2 is sufficient value for almost all the major axes of a liquid crystal molecule to arrange to 2nd direction 11b. Moreover, the 1st reset pulse P1 is a pulse for compensating direct current voltage inclining toward the DHF liquid crystal 11 by impression of the 2nd reset pulse P2; and starting, the electrical potential difference of the 1st reset pulse P1 and the 2nd reset pulse P2 has an equal absolute value, and its polarity is reverse [ the reset pulse ].

[0040] In addition, each of polarities of each [ these ] pulses P1 and P2 and electrical-potential-difference values is the polarities and electrical potential differences to the reference voltage V0 of a data signal. This reference voltage V0 is the same as the electrical potential difference impressed to a counterelectrode 7. Moreover, the pulse width of the gate pulse supplied to the gate line 5 is narrower than the pulse width of a pulse pair supplied to a data line 6. This is for holding the voltage level of the pulse in the second half of a pulse pair at accuracy in the capacity (capacity which consists of a pixel electrode 3, a counterelectrode 7, and DHF liquid crystal 11) of

each pixel. In drawing 2, in order to make a drawing legible, the difference of the pulse width of a pulse pair on a gate pulse and a data line is emphasized.

[0041] If a gate pulse turns off, a transistor 4 will also be turned off and the capacity of each pixel of - of 1st line the 8th line will hold an electrical potential difference almost equal to electrical potential difference-VR of the 2nd reset pulse P2. Supposing white (light transmission) is written in a pixel on a forward electrical potential difference and black (light impermeability) is written in a pixel on a negative electrical potential difference, all the pixels of - of 1st line the 8th line will be in a black condition (blanking) condition.

[0042] Then, the anaphase selection period of the pixel of the 1st line begins, the line driver 21 impresses a gate pulse to the gate line 5 of the 1st line, and TFT (TFT of the 1st line)4 connected to the gate line 5 of the 1st line turns it on. On the other hand, the train driver 22 impresses the write-in pulse P4 and the compensation pulse P3 which have the electrical potential difference (write-in electrical potential difference) VD corresponding to the display gradation of the pixel of the 1st line to each data line. It is a pulse for compensating that direct current voltage inclines toward the DHF liquid crystal 11 by impression of the write-in pulse P4, and the compensation pulse P3 is impressed, and an absolute value has the same electrical potential difference with the write-in pulse P4 and reversed polarity. The minimum value of the write-in electrical potential difference VD is made into an electrical potential difference V0, maximum Vmax is made into a value [ a little ] lower than the electrical potential difference VR of the 2nd reset pulse P2, it writes in in the range of V0 - Vmax, and an electrical potential difference is controlled by this example according to display gradation.

[0043] While the write-in pulse P4 is impressed to the data line 6, the line driver 21 turns off a gate pulse and turns off TFT4 of the 1st line. For this reason, as shown in drawing 1 (a), the wave of the electrical potential difference impressed to the pixel electrode 3 of the 1st line is written in with the pair of the reset pulses P1 and P2 impressed to a selection period in the first half, and the compensation pulse P3 impressed to an anaphase selection period, and serves as a pair of a pulse P4.

[0044] The capacity of each pixel of the 1st line holds the electrical potential difference currently impressed when TFT4 of the 1st line turned off, i.e., an electrical potential difference almost equal to the electrical potential difference VD of the write-in pulse P4. For this reason, the pixel of the 1st line maintains the gradation corresponding to the write-in electrical potential difference VD, i.e., the gradation corresponding to an indicative data, till the first half selection period of the following frame.

[0045] Henceforth, as the anaphase selection period of the 2nd and 3rd ... and the gate line 5 of the 8th line comes and the line driver 21 is shown in drawing 2 (b) - (d) Sequential impression of the gate pulse is carried out on the 2nd and 3rd ... and the gate line 5 of the 8th line, and the train driver 22 impresses the compensation pulse P3 and the write-in pulse P4 corresponding to an indicative data which writes in and has an electrical potential difference VD to each data line 6, as shown in drawing 2 (h). consequently, to the pixel electrode 3 of - of 2nd line the 8th line. Drawing 1 (b) the wave-like pulse signal shown in - (h) is impressed, respectively, and the capacity which is the pixel of - of 2nd line the 8th line The electrical potential difference currently impressed when TFT4 of - of 2nd line eight lines turned off, i.e., an electrical potential difference almost equal to the electrical potential difference VD of the write-in pulse P4, is held, and this maintains the gradation corresponding to an indicative data till the next first half selection period of the gate line of - of 1st line the 8th line. Above, the writing to the pixel of - of 1st line the 8th line is completed.

[0046] Then, the first half selection period of the pixel of - of 9th line the 16th line comes, and the line driver 21 impresses a gate pulse to the gate line 5 of - of 9th line the 16th line simultaneously, as shown in drawing 2 (e) - (g). On the other hand, the train driver 22 impresses the pair of the 1st reset pulse P1 and the 2nd reset pulse P2 to each data line 6. Then, the anaphase selection period of the pixel of - of 9th line the 16th line comes, and one by one, as shown in drawing 2 (e) - (g), the line driver 21 carries out sequential impression of the gate pulse on the 9th and 10th ... and the gate line 5 of the 16th line, as the train driver 22 is shown in drawing 2 (h); it writes in each data line 6 with the compensation pulse P3, and impresses a pulse P4. Consequently, the wave-like electrical potential difference pulse shown in the pixel electrode 3 of - of 9th line the 16th line at drawing 1 (a) - (h) is impressed, and the pixel of - of 9th line the 16th line maintains the gradation corresponding to an indicative data till the next first half selection period of the pixel of - of 9th line the 16th line.

[0047] Henceforth, the same actuation is repeated every eight lines, and when the writing to the pixel of all lines is completed, write-in actuation is ended. And initiation of the following frame repeats above-mentioned actuation again from the pixel of the 1st line.

[0048] The flow of the write-in whole actuation explained above comes to be shown in drawing 3 (a) - (d). In addition, drawing 3 (a) and (d) show one screen of this liquid crystal display component, and drawing 3 (b) and (c)



show eight lines-of the one screen.

[0049] First, a reset pulse pair is impressed to the pixel of – of 1st line the 8th line, and as hatching is attached and shown in drawing 3 (a), all the pixels of – of 1st line the 8th line are set as black (blank condition) (first half selection period of the pixel of – of 1st line the 8th line). Next, it writes in the pixel of the 1st line with the compensation pulse P3, and the pair of a pulse P4 is impressed, and as shown in drawing 3 (b), the pixel of the 1st line is set as the gradation corresponding to an indicative data (anaphase selection period of the pixel of the 1st line).

[0050] Next, it writes in the pixel of the 2nd line with the compensation pulse P3, and the pair of a pulse P4 is impressed, and as shown in drawing 3 (c), the pixel of the 2nd line is set as the gradation corresponding to an indicative data (anaphase selection period of the pixel of the 2nd line). Henceforth, the same actuation is repeated to the pixel of the 8th line, and the pixel of – of 1st line the 8th line is set as the gradation corresponding to an indicative data.

[0051] Then, the pair of reset pulses P1 and P2 is impressed to the pixel of – of 9th line the 15th line, and as shown in drawing 3 (d), all the pixels of – of 9th line the 15th line are set as black (blank condition) (first half selection period of the pixel of – of 9th line the 15th line). Next, it writes in the pixel electrode 3 of – of 9th line the 15th line with the compensation pulse P3, and sequential impression of the pair of a pulse P4 is carried out, and as shown in drawing 3 (b) and (c), the pixel of each line is set as the gradation corresponding to an indicative data one by one.

[0052] Henceforth, again, after the same actuation is repeated and the writing of an indicative data is completed on the whole 1 screen, as shown in drawing 3 (a), the pair of reset pulses P1 and P2 is impressed to the pixel of – of 1st line the 8th line.

[0053] According to the above-mentioned example, the pixel of a multi-line can be simultaneously set as a blanking condition. For this reason, as compared with the case where a reset pulse pair is impressed according to an individual, the write-in time amount for one screen can be shortened at the selection period of the pixel of each line. Moreover, data processing in the train driver 22 becomes easy, and can simplify the structure of the train driver 22.

[0054] Next, an example of the configuration of the line driver 21 and the train driver 22 is explained with reference to drawing 7. The train driver 22 consists of the timing signal generation circuit 31, an electrical-potential-difference generation circuit 32, a selection-signal generation circuit 33, and a selection circuitry 34. For example, the selection-signal generation circuit 33 and a selection circuitry 34 are arranged for every data line, and the timing signal generation circuit 31 and the electrical-potential-difference generation circuit 32 are arranged common to two or more data lines 6.

[0055] The timing signal generation circuit 31 generates the clock signal of for example, periodic  $\Delta t$ . The electrical-potential-difference generation circuit 32 generates two or more electrical potential differences impressed to a data line 6. The indicative data of a clock signal and a pixel unit is supplied to the selection-signal generation circuit 33. When the indicative datas of each pixel of the 1st line, the 2nd line, and ... are assumed to be  $X_1, X_2, \dots, X_8$  and  $X_9$ , and ..., the selection-signal generation circuit 33 The data  $X_R$  corresponding to the electrical potential difference  $V_R$  of a reset pulse are inserted every 8 pixels, and select data  $X_R, -X_R, -X_1, X_1, -X_2, X_2, -X_3, \dots, -X_8, X_8$  and  $X_R, -X_R, -X_9, X_9$ , and ... are generated. A selection circuitry 34 chooses the thing corresponding to select data among two or more electrical potential differences supplied from the electrical-potential-difference generation circuit 32, and supplies it to a data line 6.

[0056] On the other hand, line DORABA 21 consists of drivers 42 which impress the electrical potential difference corresponding to the output data of the scan (address) data generation circuit 41 and the scan data generation circuit 41 to the gate line 5. According to the clock signal supplied from the timing signal generation circuit 33, the scan data generation circuit 41 generates the data stream corresponding to a gate pulse, and supplies it to a driver 42.

[0057] By the above-mentioned actuation approach, gradation control of the ferroelectric liquid crystal component mentioned above was performed. In this actuation approach, for 45 microseconds, the electrical potential difference  $V_R$  of a reset pulse was set as 17V, and the write-in electrical potential difference  $V_D$  was set as  $0 \leq V_D \leq 14V$  for pulse width  $\Delta t$ . The result is shown in drawing 8. As for drawing 8 (a), the property at the time of writing in with a reset pulse pair and impressing a pulse pair to a pixel continuously and drawing 8 (b) show the property at the time of writing in after 7 selection-period ( $7\Delta t$ ) progress, and impressing a pulse pair to a pixel, after impressing a reset pulse pair like drawing 1 (h) like drawing 1 (a). A clear gradation display is possible for any case.

[0058] In addition, in order to hold the signal level on a data line as mentioned above in the capacity which becomes accuracy from the pixel electrode 3, a counterelectrode 7, and the DHF liquid crystal 11, the thing from which the signal level on a data line changes and for which a gate pulse turns off a few in front is desirable.

[0059] In addition, although the first half selection period of eight gate lines was made into the same timing in the above-mentioned example, it may not be limited to eight but two or more any are sufficient. Moreover, it is good also as separate timing, without making the first half selection period of two or more gate lines into the same timing. The selection period of one line is divided into a selection period and an anaphase selection period also in this case in the first half, a reset pulse pair is impressed to a data line 6 in the first half at a selection period, it writes in an anaphase selection period and the pair of a pulse and a compensation pulse is impressed to a data line 6.

[0060] However, if there are too many lines which share a selection period in the first half, time amount after being set as a blanking condition until it writes data in the pixel of the last line will become long too much, and the problem that a display flickers will occur. Moreover, when there are few lines which share a selection period in the first half, there is a problem that a selection period will be in a condition equal to being set up according to an individual in the first half, and the write-in time amount for one screen becomes long. Experimentally, as for the number of lines with which a line count, i.e., the number of the gate lines 5, shares a selection period the case of 200 thru/or about 400 in the first half, 6 thru/or 10, especially 8 are desirable.

[0061] In addition, although the electrical potential difference of the 1st and the 2nd reset pulse P1 and P2 is set to VR and -VR and it is impressed by the gate line in this sequence in the above-mentioned example, reverse is sufficient as the sequence of impression of the 1st and the 2nd reset pulse P1 and P2. In this case, each pixel is set as white (light transmission condition) in a selection period in the first half, after that, is an anaphase selection period and is set as the gradation corresponding to an indicative data. It is more desirable to set each pixel as a black condition in a selection period in the first half, since the sensibility of human being's eyes is more sensitive to white than black.

[0062] The reset electrical potential difference VR and -VR may not be the electrical potential differences in which the major axis (director) of the liquid crystal molecule of the DHF liquid crystal 11 carries out orientation in the directions 11a and 11b of orientation thoroughly that what is necessary is just the electrical potential difference which almost carries out orientation in the 1st or 2nd direction 11a and 11b of orientation.

[0063] Although the 1st reset pulse and the 2nd reset pulse are impressed to a pixel by a unit of 1 time in the above-mentioned example in the first half at the selection period, if the count of impression of the 1st reset pulse and the 2nd reset pulse is the same, the count of impression is arbitrary and good.

[0064] Although the ferroelectric liquid crystal display device driven in the above-mentioned example sets mostly transparency shaft 14a of one polarizing plate 14 to 2nd direction of orientation 11b of the DHF liquid crystal 11 at parallel. The above-mentioned actuation approach set mostly transparency shaft 14a of one polarizing plate 14 to 1st direction of orientation 11a of the DHF liquid crystal 11 at parallel. the time of carrying out orientation of the DHF liquid crystal 11 to 2nd direction of orientation 11b — permeability — most — being high (a display the brightest) — when carrying out orientation of the DHF liquid crystal 11 to 1st direction of orientation 11a, it can apply also to actuation of a ferroelectric liquid crystal display device with the lowest (a display most darkly) permeability. Moreover, the actuation approach of this invention is applicable not only to the ferroelectric liquid crystal display device which uses TFT as an active component but the ferroelectric liquid crystal display device which uses MIM as an active component.

[0065]

[Effect of the Invention] According to the liquid crystal display of this invention, and the actuation approach of a liquid crystal display component, as explained above, at least one side of the electrical potential difference which makes the orientation of the liquid crystal change into the 1st orientation condition to a selection period in the first half, and the electrical potential difference which changes orientation into the 2nd orientation condition is impressed to a pixel, a liquid crystal molecule is made into a fixed orientation condition, and the write-in electrical potential difference corresponding to an indicative data is impressed to a pixel after that at an anaphase selection period. Therefore, a clear gradation display can be made to perform to the ferroelectric liquid crystal display device of an active matrix using a non-memory nature ferroelectric liquid crystal (DHF liquid crystal) with a spiral pitch smaller than substrate spacing. Moreover, write-in time amount of the 1 field can be shortened by carrying out the first half selection period of two or more gate lines in common.

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[Translation done.]

**\* NOTICES \***

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1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. \*\*\*\* shows the word which can not be translated.
3. In the drawings, any words are not translated.

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**DESCRIPTION OF DRAWINGS**

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**[Brief Description of the Drawings]**

**[Drawing 1]** (a) - (h) is a timing chart which shows the wave of the electrical potential difference impressed to the pixel of - of Kth line the K+7th line by the actuation approach of the liquid crystal display component concerning one example of this invention.

**[Drawing 2]** (a) The timing chart which shows the wave of the electrical potential difference impressed to the gate line of - of 1st line the 16th line by the actuation approach of the liquid crystal display component which - (g) requires for one example of this invention, and (h) are timing charts which show the wave of the electrical potential difference impressed to a data line.

**[Drawing 3]** It is drawing showing the write-in procedure by this example, and drawing in which (a) and (d) show one screen, (b), and (c) are drawings showing the pixel for eight lines.

**[Drawing 4]** It is the sectional view showing the structure of the liquid crystal display component driven by the actuation approach of the liquid crystal display component concerning one example of this invention.

**[Drawing 5]** It is the top view showing the configuration of the bottom substrate of the liquid crystal display component shown in drawing 4.

**[Drawing 6]** It is drawing showing the relation of the direction of the method of \*\* of the transparency shaft of a polarizing plate, and a liquid crystal molecule, and (a) is drawing in which the transparency shaft orientation of a top substrate and (b) show the direction of the method of \*\* of a liquid crystal molecule, and (c) shows the transparency shaft orientation of a bottom substrate, respectively.

**[Drawing 7]** It is the block diagram showing an example of the configuration of a line driver and a train driver.

**[Drawing 8]** It is the graph which shows change of applied voltage and permeability.

**[Description of Notations]**

1 Transparence Substrate (Bottom Substrate)

2 Transparence Substrate (Top Substrate)

3 Pixel Electrode

4 Active Component (T.F.T.)

5 Gate Line (Scan Line)

6 Data Line (Gradation Signal Line)

7 Counterelectrode

8 Orientation Film

9 Orientation Film

10 Sealant

11 Ferroelectric Liquid Crystal (DHF Liquid Crystal)

12 Gap Material

13 Polarizing Plate (Bottom Polarizing Plate)

14 Polarizing Plate (Top Polarizing Plate)

21 Line-Driver (Line-Actuation Circuit)

22 Train Driver (Train Actuation Circuit)

31 Timing Signal Generation Circuit

32 Electrical-Potential-Difference Generation Circuit

33 Selection-Signal Generation Circuit

34 Selection Circuitry 34

41 Scan Data Generation Circuit

42 Driver

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[Translation done.]